IT IS CLAIMED:

1. A non-volatile memory system, comprising:
an array of non-volatile memory cells divided into at least two sub-arrays wherein data are simultaneously accessible in each of the at least two sub-arrays, and
data stored within the at least two sub-arrays with at least first and second different interleaving arrangements.

2. The memory system of claim 1, wherein the data simultaneously accessible in each of the at least two sub-arrays include sectors of data, and wherein sectors of data stored within the at least two sub-arrays include:

at least a first set of data sectors identified by a first set of contiguous logical addresses interleaved across said sub-arrays according to the first interleaving arrangement, and

at least a second set of data sectors identified by a second set of contiguous logical addresses interleaved within a single one of the at least two sub-arrays according to the second interleaving arrangement.

3. The memory system of claim 2, wherein indications of the degree of interleaving of sectors of stored data are also stored.

4. The memory system of claim 3, wherein the indications of the degree of interleaving are stored as overhead within the sectors of stored data to which they pertain.

5. The memory system of claim 3, wherein the indications of the degree of interleaving are stored in sectors separate from the sectors of stored data to which they pertain.

6. A method of operating a non-volatile memory system that logically links a block individually a plurality of memory cell sub-arrays

7. In a non-volatile memory having a plurality of memory cell sub-arrays that are simultaneously accessible for programming units of data thereto and reading data therefrom in

parallel, the individual sub-arrays being divided into blocks of a minimum number of memory cells that are simultaneously erasable, a method of operating the memory, comprising:

receiving a command for programming into the memory a specified number of units data less than a total data storage capacity of one block in each of the plurality of sub-arrays and having sequential logical addresses,

receiving the specified number of units of data to be programmed, and

programming the received units of data with their sequential logical addresses arranged in order across blocks of one or more of the plurality of memory cell sub-arrays according to the specified number of units of data being programmed relative to the total data storage capacity of one block in each of the sub-arrays.

8. A method of operating a non-volatile memory system, comprising:

operating the memory with data being written and read with each of at least a first degree of parallelism and a second degree of parallelism,

observing data write requests received by the memory system, and

writing data accompanying individual ones of the received write requests with one of said at least first and second degrees of parallelism in response to at least one characteristic of the received write requests.

9. The method of claim 8, wherein said at least one characteristic includes an amount of data received with a write request to be written into the memory.

10. In a flash memory system having an array of non-volatile memory cells arranged in blocks as a unit of erase, pages therein as a unit of data programming and reading, and planes of a plurality of blocks that are independently accessible, a method of operation, comprising:

logically forming metablocks that individually include a block from a plurality of the planes,

sequentially receiving write commands with varying amounts of data, and

variously writing the received data in parallel either sequentially into pages within individual blocks of one of the planes or in parallel into pages within two or more blocks of one of the metablocks in response to varying characteristics of the host write commands.

11. The method of claim 10, additionally comprising writing an indication at the same time as the received data that identifies the blocks into which the data are being written in parallel.

12. In a non-volatile memory system having an array of memory cells organized into blocks of cells that are erasable together and which individually store a plurality of units of data, a method of responding to a series of write commands that individually designate a logical address of one or more units of data to be written and which are accompanied by the designated one or more units of data being received sequentially, comprising:

converting the logical address of an individual write command into a physical address within one or more of the blocks of memory cells that allow writing the accompanying one or more units of data in parallel, wherein a number of said one or more blocks are selected for receiving said one or more units of data as a function of the number of units of data specified by at least one of the received series of write commands, the number of units of data specified by the received series of write commands varying, and

writing the selected one or more units of data into said one or more blocks in parallel.

13. A method of operating a non-volatile memory array of memory cells, comprising:
storing data with first and second different interleaving arrangements, and

in response to receiving a command to update at least some of the data stored with the first interleaving arrangement that would result in more optimal performance characteristics by being stored with the second interleaving arrangement,

reading data stored with the first interleaving arrangement, and

writing the read data and the updated data into the memory array with the second interleaving arrangement.